HIGH DENSITY AREA ARRAY SOLDER MICROJOINING INTERCONNECT STRUCTURE AND FABRICATION METHOD

This application is a Continuous of 10/052,620 filed on 01/18/2002, PAT. 6,661,098.

FIELD OF THE INVENTION

This invention pertains to the field of microelectronics, and more particularly to the field of fabricating and interconnecting extremely small semiconductor devices, commonly referred to as "chips."

RELATED INVENTIONS

The present invention is related to certain inventions assigned to the assignee of the present invention. These are disclosed in co-pending applications YOR920010249US1 and YOR920010217US1.

BACKGROUND OF THE INVENTION

Increased levels of integration in the silicon transistor technology over the last two decades have facilitated the migration from large scale integrated (LSI) to very large scale integrated (VLSI) and now to ultra-large scale integrated (ULSI) circuits for use in silicon chips for computing, communication and micro controller applications. Optimum utilization of these highly integrated silicon chips requires a more space efficient packaging with supporting devices such as memory chips. Further, with the advent of mobile communication devices, hand held organizers and computing devices, there has also been a push to integrate such varied functions into a single compact system. This in turn has led to the push in the microelectronics industry towards system-on-a-chip (SOC) approach.

Simply stated, the SOC approach attempts to integrate as many of these different device functionalities on the same silicon chip so that a single large chip can provide a variety of functions to the end user. Although conceptually very attractive, such an approach is practically daunting